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A Compact Model for Circuit Simulation of TFT-LCD Panel

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In this paper, we report a novel compact SPICE model for circuit simulation of LCD-TVs. In this work, we generated a SPICE model for a unit cell of TFT-LCD by taking all of parasitic capacitances and resistances into account. In order to extract circuit model from a unit cell, an electrical connectivity of resistors and capacitors was generated through the pattern analysis data including electrode and port data, followed by the calculation of the parasitics using a finite element method (FEM). Moreover, we employed a piecewise linear voltage-controlled capacitor model with calculated values in order to take voltage dependency of LC capacitance into account. Consequently, we generated a new kickback model which considers the influence of adjacent bus lines.

Keywords: finite element method; liquid crystal display; simulation; SPICE model

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I. INTRODUCTION

In the LCD-TV panel design, one of most critical problem is the ΔV_p problem which is caused by a capacitive coupling between the pixel and the TFT as well as the gate and data bus lines because ΔV_p is the main factor of gray level error [1]. Therefore, many efforts have been made to resolve ΔV_p problem [2–3]. However, since ΔV_p depends on the capacitance variation of liquid crystal and the signal fluctuation of neighboring data and gate lines, the amount of ΔV_p at each pixel is different from one to another.

Furthermore, since the resolution and the color depth of LCD-TV as well as the panel size increase, the row line time becomes shorter while capacitive and resistive loads of data and gate lines become larger. Therefore, interconnect effects of data and gate bus lines in the panel are critically important in the design and verification of its unit cell, and the characterization of parasitic elements such as coupling capacitance and resistance as well as the analysis of the optical properties of TFT-LCDs become fundamental to LCD panel synthesis and optimization [4].

In this paper, we report the incorporation of an accurate compact SPICE model for a unit cell of LCD-TV in order to characterize the ΔV_p problem and electrical properties of the whole panel.

II. EXTRACTION OF SPICE NET-LIST

Figure 1 shows a schematic diagram illustrating the workflow of extracting the SPICE model. Our approach is comprised of the following steps:

(1) Importing GDSII standard layout file and adding pattern analysis information;
(2) Generating electrical connectivity with the given pattern analysis information;
(3) Generating three-dimensional mesh structure with the process information;
(4) Calculating parasitic numerically by finite element method (FEM); and
(5) Generating SPICE model for unit cell based on the electric connectivity with the calculated parasitic and an additional TFT model.

In step (1), pattern analysis information is required to generate the electrical connectivity, and it consists of port and electrode information. Conductors which were connected electrically could be defined as the same electrode by the electrode name, and each electrode is able

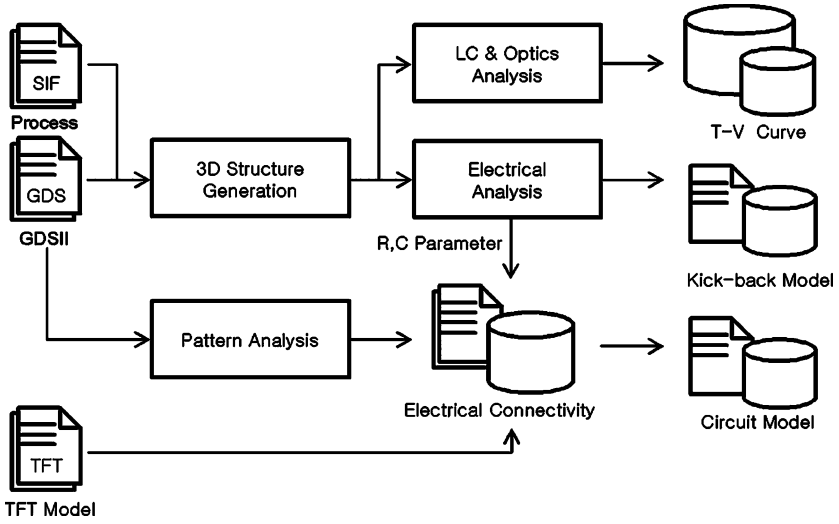


FIGURE 1 Schematic diagram illustrating the workflow for extracting SPICE model.

to include port information for input/output port. The electrode which has m ports can be modeled as $m(m-1)/2$ resistors and total electrodes which have n ports can be modeled as $n(n-1)/2$ capacitors. Specially, an electrode which has no port information is considered as a port without any resistor components.

Figure 2 shows a schematic view of exemplary layout with electrode and port information and its electrical connectivity. Referring to Figure 2(a), the exemplary layout includes a total 3 of electrodes (A, B, C) which has 3 ports (1, 2, 3 in A), 2 ports (4, 5 in B) and 1 port (6 in C), respectively. Therefore, it was modeled as an equivalent circuit of 4 resistors and 15 capacitors. In order to calculate the value of the parasitics, we have to solve the Erickson-Leslie equation and Laplace equations in the dielectric and conductor domain by the finite element method, respectively. Thereafter, all of parasitic elements are calculated by using energy method [5].

The inputting process in a text-based mesh generation to solve the problem is extremely time consuming and subject to error. Therefore, we developed graphic user interface and polygon-based solid modeling algorithm for automatic mesh generation which can take the taper angle and the conformal surface caused by process into account. Figure 3 shows the generated 3D structure by our solid modeling algorithm.

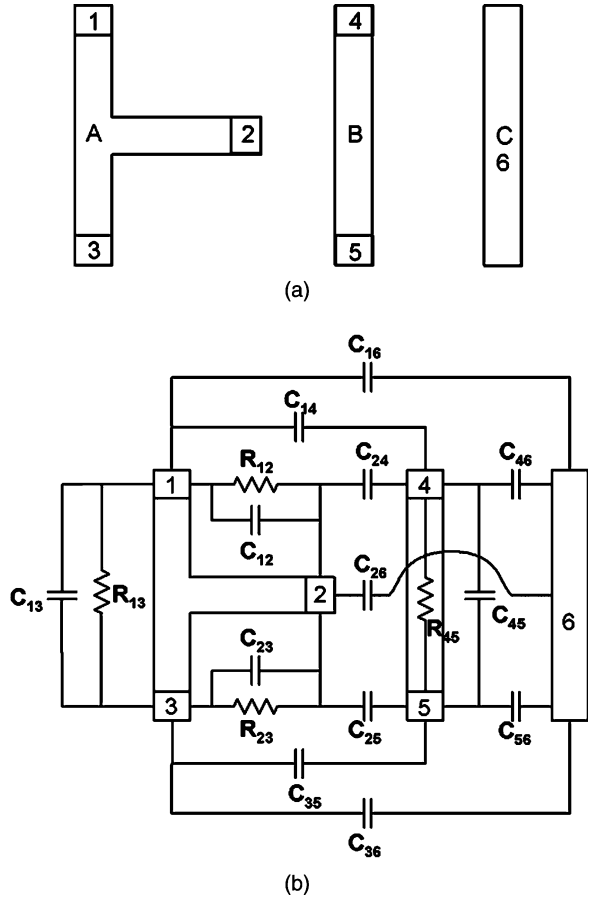


FIGURE 2 Schematic view of (a) exemplary layout with electrode and port information and (b) its electrical connectivity of resistors and capacitors.

III. RESULTS AND DISCUSSION

Figure 4 shows an exemplary cell layout and its equivalent circuit with some major parasitic elements which strongly influence the amount of ΔV_p. Referring to Figure 4, the unit cell structure includes a total of 7 electrodes and 14 ports comprising two data lines, two gate lines, storage, pixel and common electrode. Therefore, there are 91 capacitances and 9 resistances. Specially, in order to take the coupling effect of neighbor bus lines into account on one cell simulation, we included two data lines and two gate lines within a cell size.

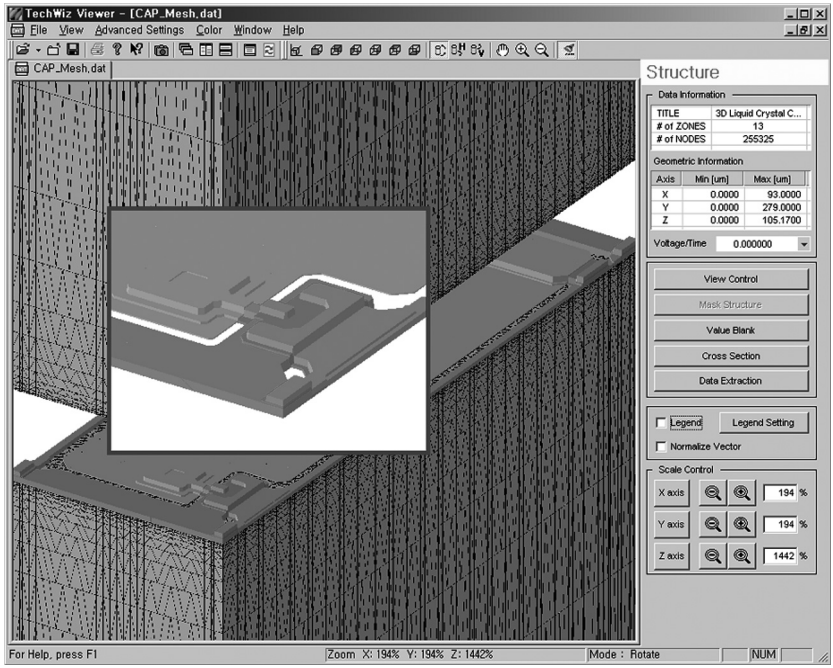


FIGURE 3 Generated 3D structure taken into account the taper angle and conformal surface.

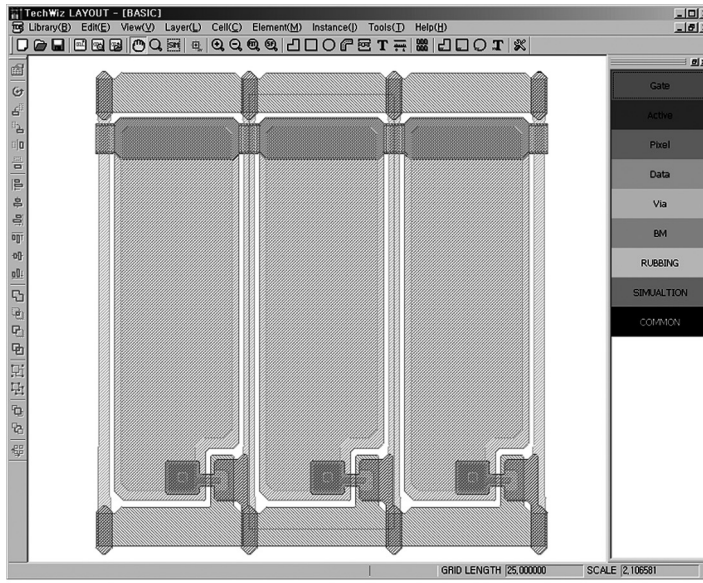
Using the equivalent circuit shown in Figure 4(b), the ΔV_p was expressed by charge conservation rule. The total electric charge of pixel electrode under ON state and OFF state of TFT can be expressed as:

$$\begin{aligned} Q_p^{\text{on}} = (C_{LC}^{\text{on}} + C_{ST}^{\text{on}}) \cdot (V_p' - V_{com}) + (C_{gdi}^{\text{off}} + \frac{C_g}{2} + C_{GP1}) \cdot (V_p' - V_{GH}) \\ + C_{DP1} \cdot (V_p' - V_{D1})\, C_{GP2} \cdot (V_p' - V_{G2}) + C_{DP2} \cdot (V_p' - V_{D2}) \end{aligned} \quad (1)$$

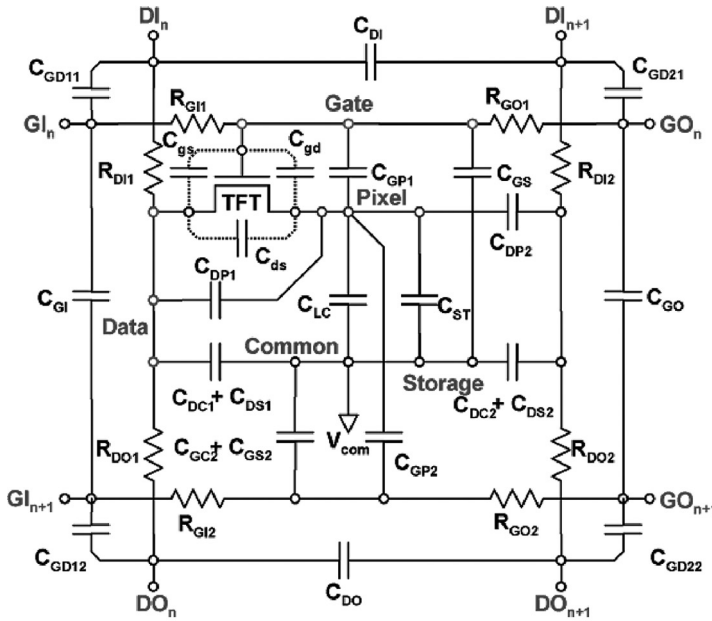
$$\begin{aligned} Q_p^{\text{off}} = (C_{LC}^{\text{off}} + C_{ST}^{\text{off}}) \cdot (V_p' - V_{com}) + (C_{gdi}^{\text{off}} + C_{GP1}) \cdot (V_p' - V_{GL}) \\ + C_{DP1} \cdot (V_p' - V_{D1}) C_{GP2} \cdot (V_p' - V_{G2}) + C_{DP2} \cdot (V_p' - V_{D2}) \end{aligned} \quad (2)$$

In the Equations (1) and (2), V_p and V'_p are the pixel voltage under ON state and OFF state, V_{GH} and V_{GL} is ON state and OFF state gate voltage of TFT, respectively. V_{com} and V_{D1}, V_{G2}, V_{D2}, is the common voltage and the signal voltage of each bus line, respectively. According to the law of conservation of electric charge

$$Q_P^{\text{on}} = Q_P^{\text{off}} \quad (3)$$



(a)



(b)

FIGURE 4 Exemplary (a) layout of unit cell and (b) its equivalent circuit with some major parasitics.

and the definition of the kick-back voltage,

$$V_p' = V_p - \Delta V_p \tag{4}$$

ΔV_p can be expressed as follows:

$$\Delta V_p = \Delta V_p' + \Delta V_{PG1} + \Delta V_{PD1} + \Delta V_{PG2} + \Delta V_{PD2} \tag{5}$$

In Equation (5), ΔV_p consists of five terms. The first term represents effect of channel capacitance of TFT and LC capacitance, and the other terms represent effect of neighbor bus lines. Each term of Equation (5) can be expressed by Equations (6–10).

$$\Delta V_p' = \frac{(C_{LC}^{\text{on}} - C_{LC}^{\text{off}} + C_{ST}^{\text{on}} - C_{ST}^{\text{off}}) \cdot (V_{com} - V_p) + \frac{1}{2} C_g \cdot (V_{GH} - V_p)}{(C_{LC}^{\text{off}} + C_{ST}^{\text{off}} + C_{gd}^{\text{off}} + C_{GP1} + C_{DP1} + C_{GP2} + C_{DP2})} \tag{6}$$

$$\Delta V_{PG1} = \frac{(C_{gd}^{\text{off}} + C_{GP1}) \cdot \Delta V_{G1}(t)}{(C_{LC}^{\text{off}} + C_{ST}^{\text{off}} + C_{gd}^{\text{off}} + C_{GP1} + C_{DP1} + C_{GP2} + C_{DP2})} \tag{7}$$

$$\Delta V_{PD1} = \frac{C_{DP1} \cdot \Delta V_{D1}(t)}{(C_{LC}^{\text{off}} + C_{ST}^{\text{off}} + C_{gd}^{\text{off}} + C_{GP1} + C_{DP1} + C_{GP2} + C_{DP2})} \tag{8}$$

$$\Delta V_{PG2} = \frac{C_{GP2} \cdot \Delta V_{G2}(t)}{(C_{LC}^{\text{off}} + C_{ST}^{\text{off}} + C_{gd}^{\text{off}} + C_{GP1} + C_{DP1} + C_{GP2} + C_{DP2})} \tag{9}$$

$$\Delta V_{PD2} = \frac{C_{DP2} \cdot \Delta V_{D2}(t)}{(C_{LC}^{\text{off}} + C_{ST}^{\text{off}} + C_{gd}^{\text{off}} + C_{GP1} + C_{DP1} + C_{GP2} + C_{DP2})} \tag{10}$$

The turn-on time of gate signal is negligible because its interval is relatively short. Hence, the Equation (5) can be expressed with the Equation (11)

$$\Delta V_p = \Delta V_p^{DC} + \Delta V_p^{AC} \tag{11}$$

$$\Delta V_p^{DC} = \frac{\begin{array}{c}(C_{LC}^{\text{on}} - C_{LC}^{\text{off}} + C_{ST}^{\text{on}} - C_{ST}^{\text{off}}) \cdot (V_{com} - V_p) + \frac{1}{2} C_g \cdot (V_{GH} - V_p) \\ + (C_{gd}^{\text{off}} + C_{GP1} + C_{GP2}) \cdot V_{GL}\end{array}}{(C_{LC}^{\text{off}} + C_{ST}^{\text{off}} + C_{gd}^{\text{off}} + C_{GP1} + C_{DP1} + C_{GP2} + C_{DP2})} \tag{12}$$

$$\Delta V_p^{AC} = \frac{C_{DP1} \cdot \Delta V_{D1}(t) + C_{DP2} \cdot \Delta V_{D2}(t)}{(C_{LC}^{\text{off}} + C_{ST}^{\text{off}} + C_{gd}^{\text{off}} + C_{GP1} + C_{DP1} + C_{GP2} + C_{DP2})} \tag{13}$$

Figures 5 and 6 are plots showing the result of SPICE simulation with the influence of parasitic capacitances on the ΔV_p. We used Level 40 HP a-Si model for the SPICE model of TFT [6]. The calculated LC capacitance as a function of RMS voltage between pixel and common electrodes was modeled by the piecewise linear voltage-controlled capacitor as shown in Equation (14).

```
Glc pixel common    VCCAP PWL(1)    pixel common    (14)
+-6.50,0.839843p, -6.00,0.831120p, -5.50,0.818794p, -5.00,0.800529p,
+-4.50,0.771693p, -4.00,0.725919p, -3.50,0.660901p, -3.00,0.574530p,
+-2.50,0.470439p, -2.00,0.458021p, -1.50,0.456107p, -1.00,0.455356p,
+-0.50,0.455022p,  0.00,0.454946p,  0.50,0.455022p,  1.00,0.455356p,
+1.50,0.456107p,   2.00,0.458021p,  2.50,0.470439p,  3.00,0.574530p,
+3.50,0.660901p,   4.00,0.725919p,  4.50,0.771693p,  5.00,0.800529p,
+5.50,0.818794p,   6.00,0.831120p,  6.50,0.839843p
```

Other parasitic capacitances should also be considered as voltage-dependent capacitor because the director of an LC tends to move in a different

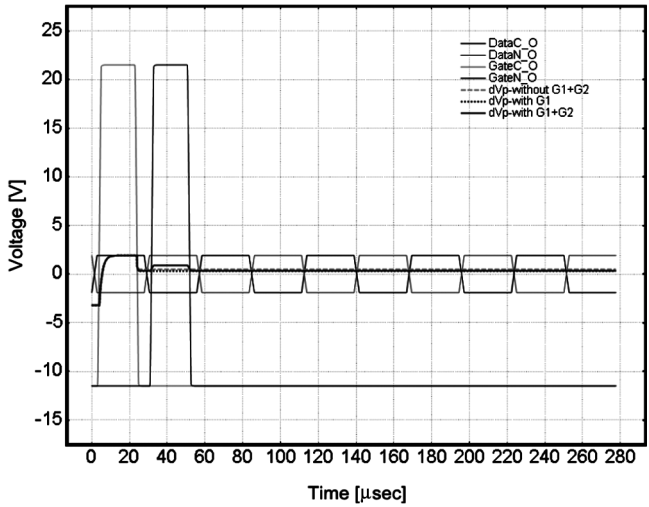


FIGURE 5 Influence of gate signal which affect the pixel voltage drop (dotted line: without C_{GP1} and C_{GP2}, two dotted line: with C_{GP1}, solid line: with C_{GP1} and C_{GP2}).

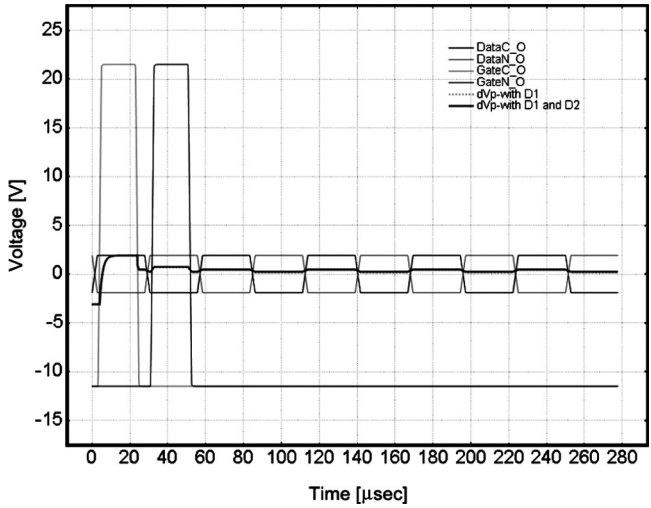


FIGURE 6 Influence of data signal which affect the pixel voltage drop (dotted line: with C_{GP1}, solid line: with C_{GP1} and C_{GP2}).

manner under each voltage condition. However, since the variations are less than 0.1% of their maximum values in this work, the parametric values were assumed to be fixed.

Figure 5 is a schematic diagram illustrating the influence of the gate signal on the pixel voltage drop. Referring to Figure 5, we can observe that the gate1-pixel capacitance C_{GP1} increases by an amount of ΔV_p while the gate-to-pixel capacitance C_{GP2} decreases by an amount of ΔV_p. Furthermore, the signal at the pixel electrode is ascending within turn-on period of the next gate signal. However, since the turn-on time of the gate signal is relatively very short, this effect can be neglected. Therefore, we can take the gate-pixel capacitances as a DC level shifter with an amount of ΔV_p.

Figure 6 is another schematic diagram showing the influence of data signal on the pixel voltage drop. Referring to Figure 6, we can note that the signal of the adjacent data line is fluctuating by the amount of ΔV_p, and since we assumed the column inversion mode as a driving method, the data1-pixel capacitance and the data-to-pixel capacitance compensate their fluctuation effectively. However, in this simulation, there still remains the fluctuation of ΔV_p under the fully compensated condition because of the difference of the data1-pixel capacitance and the data-to-pixel capacitance caused by asymmetric shape of pixel electrode.

IV. CONCLUSION

In this paper, we report a novel compact SPICE model for circuit simulation of LCD-TVs. We generated a SPICE model for a unit cell of TFT-LCD by taking all of parasitic capacitances and resistances into account. In order to extract a circuit model of unit cell, we generated electrical connectivity of resistors and capacitors by the pattern analysis information comprising electrode and port information. Thereafter, we calculated the parasitic elements with a finite element method (FEM). In order to take the voltage dependency of LC capacitance into account, we used a piecewise linear voltage-controlled capacitor model. We generated a new kickback model which can take the influence of neighboring bus lines into account. According to our new model, ΔV_p consists of two terms wherein the first term represents DC part of the ΔV_p from the gate signal of TFT and the second term represents the AC part of the ΔV_p from the voltage fluctuation of the data signal caused by image data and the driving method.

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